ABSTRACT OF THE DISCLOSURE

The present invention proposes an ESD protection circuit with low input capacitance, suitable for an I/O pad. The ESD protection circuit includes a plurality of diodes and a power-rail ESD clamp circuit between power lines. The diodes are stacked and coupled between a first power line and the I/O pad. The ESD protection circuit between power lines is coupled between the first power line and a second power line. During normal operation, the diodes are reverse-biased and the ESD protection circuit between power lines is turned off. When an ESD event between the power line and the I/O pad occurs, the diodes are forward-biased, and the ESD protection circuit between power lines is turned on to conduct ESD current. The equivalent input capacitance of the ESD protection circuit of the present invention is very small, making it particularly suitable for the I/O port of high-frequency or high-speed IC.